IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

PROFESSOR MASAHIRO IIDA, *Plaintiff*, v. INTEL CORPORATION, *Defendant*.	Case No. 6:22-cv-00662-ADA Jury Trial Demanded

INTEL'S REPLY CLAIM CONSTRUCTION BRIEF

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The following exhibits are attached to the Supplemental Declaration of Heather E. Takahashi, submitted concurrently herewith.

Exhibit	Description
19	"FPGA Architecture, Altera White Paper WP-01003-1.0" (July 2006), available at www.altera.com/en_US/pdfs/literature/wp/wp-01003.pdf
20	Plaintiff's Disclosure of Asserted Claims and Preliminary Infringement Contentions, served September 20, 2022

I. INTRODUCTION

Iida ostensibly disputes Intel's proposed constructions for "look up table of M inputs and N outputs" and "LUT units." But he offers little in the way of meaningful opposition.

First, as Intel's opening brief explained, the '737 patent expressly defines a "look up table of M inputs and N outputs." Iida does not dispute the substance of Intel's construction, which is necessary to explain a technical concept to the lay jury. He also fails to engage with the clear language used in the patent. The Court should reject Iida's arguments and construe this term consistent with its undisputed meaning and the patent's clear definition.

Second, as Intel's opening brief explained, the plain meaning of "LUT units" renders the asserted claims indefinite because a single embodiment can both infringe and not infringe simultaneously. "That is the epitome of indefiniteness." *Geneva Pharms., Inc. v. GlaxoSmithKline PLC*, 349 F.3d 1373, 1384 (Fed. Cir. 2003). Iida complains that Intel omitted "implementation details" in crafting its illustration of a device that both meets and does not meet the language of the claims simultaneously. But the lack of detail in Intel's example is ***exactly*** the point: Intel's example contains every detail about "LUT units" required by the claim language—and Iida has not identified any specific structure he believes is missing—yet it is still impossible to assess infringement. This is true whether or not the "LUT units" must be irreducible, as Iida argues. But even if that construction mattered, it is an unsupported attempt to rewrite the claim language.

II. CONSTRUCTION OF THE DISPUTED CLAIM TERMS

A. "look up table of M inputs and N outputs"

Iida concedes that, pursuant to its plain and ordinary meaning, a "look up table of M inputs and N outputs" must be "composed of memories" and "capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs." Iida basically recites Intel's definition in his brief, explaining that a look up table is a "digital memory" and that a look up table "having k inputs

requires 2^k memory bits." Dkt. 54 at 6, 7 (emphasis added); *see also* Dkt. 51-1 (Melvin Decl.) ¶ 40 (explaining how a look up table with 2^K bits can implement any function of K inputs).[1]

Iida nevertheless maintains that the term "look up table of M inputs and N outputs" does not require construction. However, the construction of a claim term is proper if "the explanation aids the court and the jury in understanding the term as it is used in the claimed invention." *Funai Elec. Co. v. Daewoo Elecs. Corp.*, 616 F.3d 1357, 1366 (Fed. Cir. 2010). While jurors may be familiar with the idea of looking up information in a table, the parties agree that in the context of a programmable logic device the term "look up table" has a specific technical meaning. *See* Dkt. 51-1 ¶¶ 36–43 ("A look up table[] is a 'digital memory' that can implement a logic function by storing the values for that function's truth table in its memory," and "a look up table with at 2^K bits can implement any *K*-input 1-output logic function."); Dkt. 54-3 ¶¶ 21, 23 ("A look up table is a 'digital memory' that can implement a logic function by storing the values for that function's truth table in its memory cells," and "a LUT having k inputs requires 2^k memory bits."). For example, without a construction, the jury might incorrectly assume that a "look up table of M inputs and N outputs" must be able to perform an arbitrary function of M inputs on ***each*** of its N outputs or need not be able to perform any arbitrary function of its inputs ***at all***. Neither party appears to advocate for these positions, which would be inconsistent with the intrinsic evidence. *See* Dkt. 51-1 ¶¶ 52–53. To avoid such confusion and aid the jury, the Court should construe this term and, in particular, it should adopt the undisputed understanding of "look up table of M inputs and N outputs."

[1] Iida also contends that the "look up table of M inputs and N outputs" need not be part of a programmable logic circuit device. This is immaterial, and Intel is willing to resolve this aspect of the parties' dispute by construing a "look up table of M inputs and N outputs" to mean a "component that is composed of memories and is capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs."

That construction also comports with the written description of the patent, where the patentee expressly defined "look up table of M inputs and N outputs." *See* '737 patent at 1:25–28, 1:46–54. Although Iida contends that the definitional language in the specification is merely "describ[ing] LUT nomenclature" and does not satisfy the "exacting" standard for lexicography (Dkt. 54 at 12–13), he never explains why these passages—which define what a "look up table of M inputs and N outputs" ***is*** and not simply what it "might be" or "could be"—do not amount to a clear definition. Nor does he engage with the Federal Circuit's clear guidance on claim construction. *See Kyocera Senco Indus. Tools Inc. v. Int'l Trade Comm'n*, 22 F.4th 1369, 1378 (Fed. Cir. 2022) (holding that the patentees clearly defined "driven position" in the written description by stating "[t]his bottom position is also sometimes referred to herein as the 'driven position'"); *see also C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004) ("[T]he inventor's written description of the invention, for example, is relevant and controlling insofar as it provides clear lexicography.").

Instead, Iida contends that a patentee's express definition of a term is binding only if it ascribes a "novel" definition to the term—not if it ascribes a definition that is consistent with the customary usage of the term. Dkt. 54 at 13. But no case stands for such a proposition. The primary case Iida cites for this rule, *Uniloc*, is inapposite. In that decision, the magistrate judge contrasted a patentee's failure to define one term against the patentee's conscious choice to define ***other terms*** in the written description. *Uniloc Luxembourg S.A. v. Corel Inc.*, No. 6:12-CV-968, 2014 WL 7141821, at *8 (E.D. Tex. Dec. 15, 2014). Essentially, the court held that the patentee knew how to effect a clear lexicography for one term, but chose not to do so for certain other terms. *Id.* The court never rejected an express definition simply because it was consistent with the plain and ordinary meaning of the defined term.

Iida's other cases (Dkt. 54 at 13) simply articulate the generic rule that, if patentees seek to depart from the plain and ordinary meaning of a term, they must effect a clear lexicography or disclaimer. *See, e.g.*, *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003) ("We indulge a heavy presumption that claim terms carry their full ordinary and customary meaning, . . . unless the patentee unequivocally imparted a novel meaning to those terms or expressly relinquished claim scope during prosecution.") (cleaned up). Here the "heavy presumption" in favor of customary meaning actually ***supports*** Intel's proposed construction, which Iida concedes is consistent with the ordinary meaning of the term "look up table of M inputs and N outputs." *See* Dkt. 54 at 14. It does not follow from this presumption in favor of customary meaning that, if a patentee expressly ascribes a definition to a term that is consistent with the customary meaning, the Court should decline to construe the term.

In sum, Iida offers no meaningful opposition to Intel's proposed construction. For the reasons Intel explained in its opening brief, a "look up table of M inputs and N outputs" should be construed as "a component that is composed of memories and is capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs."

B. "LUT units"

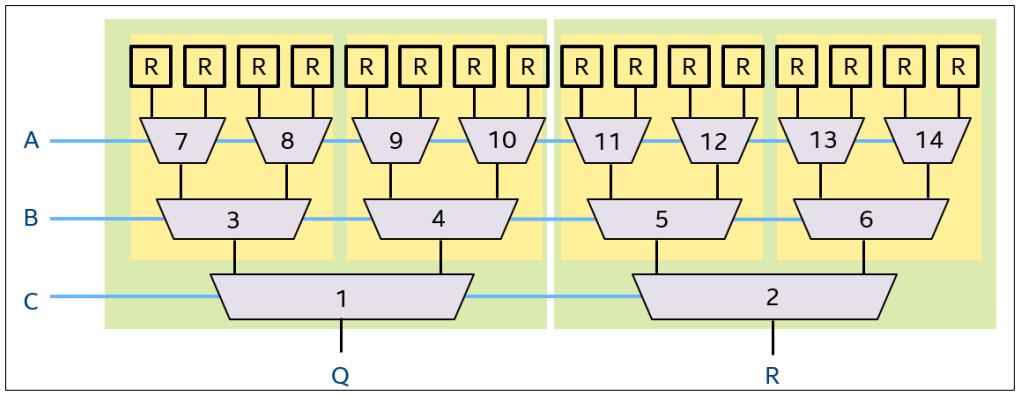
Iida's arguments highlight the very reason why the asserted claims are indefinite in light of the ordinary meaning of "LUT units." Using Iida's own words, it is the ***claims*** (not Intel's figures) that fail to "provide enough detail to a person of ordinary skill in the art to determine whether" certain structures in a given look up table "represent individual LUT units." Dkt. 54 at 19. Without those details, the claim language allows multiple ways of identifying the "LUT units" in a single device, only some of which infringe. "That is the epitome of indefiniteness." *Geneva*, 349 F.3d at 1384. Recognizing this fact, Iida tries to import a limitation into the claims in an effort to preserve their validity. Dkt. 54 at 15, 17. He claims LUT units are "irreducible," meaning they

"cannot be fractured or divided into smaller LUT units." *Id.* at 17. But nothing in the plain meaning of "LUT units" or the specification supports such a limitation. And even if "LUT units" must be irreducible, the claims are still indefinite.

1. Iida's Arguments Confirm the Indefiniteness of the Claims

Iida faults Intel for omitting key implementation details necessary to assess infringement, characterizing Intel's examples as "simplified block diagrams" that do not show "how the look up table itself is actually *implemented*." Dkt. 54 at 5. He also suggests that a skilled artisan "would easily identify a LUT unit given sufficient information about the design of a given look up table." *Id.* at 19. After all, Iida explains, the '737 patent "is about the implementation, architecture, configuration, and construction (i.e., build) of circuits." *Id.*

But this argument just confirms Intel's point: ***nothing in the claims*** explains how to identify the LUT units in a particular device. Intel's example implementation—a single, physical device—captures this fact about the claims:



Dkt. 51 at 12. This figure has all the details necessary to assess indefiniteness. As explained in Intel's opening brief, this figure depicts a device with a 16-bit memory array connected to a tree of multiplexers, with three inputs (A, B, and C) and two outputs (Q, R). Dkt. 51 at 9–12. The figure therefore depicts a "look up table of M inputs and N outputs" as required by the preamble of claim 1 of the patent. Depending on how one maps the term "LUT units" onto this ***single*** device, it may

have two "LUT units" (green boxes) with no "selectors selecting I/O signals of said plurality of LUT units" (as required by independent claims 1 and 7), or it may have four "LUT units" (yellow boxes) with two "selectors selecting I/O signals of said plurality of LUT units," namely selectors 1 and 2. And there is no reason (and Iida has articulated no reason) why, based on ***the language of the claims***, a skilled artisan would choose one mapping over another. Assessing whether this device meets those claim limitations is a wholly "arbitrary" exercise, as Iida himself recognizes. This is ultimately a problem with Iida's claims, not with Intel's figures, which illustrate the configuration of actual programmable logic devices.

It is telling that, while Iida faults Intel for purportedly oversimplifying its example, he never points to any specific implementation details that Intel omitted—let alone any claim language that requires such implementation details. This handwaving is inadequate to lend definiteness to claim language. If it were sufficient, the definiteness requirement would be vitiated: any patentee could have an expert say "I know it when I see it" and, as a result, avoid invalidity. This is far from the "clear notice of what is claimed" that is required. *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 899 (2014).

Iida's argument that a "LUT unit" must be "unitary" or "irreducible" fails for the same reason. Iida has not identified a single detail a skilled artisan would use to assess whether a particular "LUT unit" is irreducible—let alone details supported by claim language. Nor could he identify those details if he tried. The concept of an "irreducible" circuit component is nonsensical. Circuit components are, by their very nature, an abstraction. A "logic gate" is an abstract way of describing a group of "physical transistors" that implement fundamental logic function on binary inputs. Dkt. 51-1 (Melvin Decl.) ¶ 34. A "digital memory" is an abstract way of describing a collection of memory cells and selectors, each of which are themselves collections of physical

transistors. *See id.* ¶ 36. And a "look up table" is an abstract way of describing a digital memory than can implement certain logic functions. *Id.* ¶¶ 36–41. There is no magic "unitary" element that is "irreducible." Ultimately, everything in a circuit is "reducible" down to a sea of transistors deposited on silicon. A skilled artisan, therefore, could divide Intel's example into its individual transistor components and ***still*** not be capable of identifying "details" that make one set of transistors an "irreducible" LUT unit and another set of transistors a "reducible" LUT unit.

Ultimately, the "LUT units" in Intel's example can be identified in multiple ways, each of which is consistent with the claim language. This is problematic because it means the same device could both "simultaneously infringe and not infringe the claims" based on unclaimed conditions. *Geneva*, 349 F.3d at 1384. As a result, under well-established precedent, the claims are indefinite. *See Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 789 F.3d 1335, 1341 (Fed. Cir. 2015).

2. Nothing in the Specification Requires the Claimed "LUT Units" To Be Irreducible.

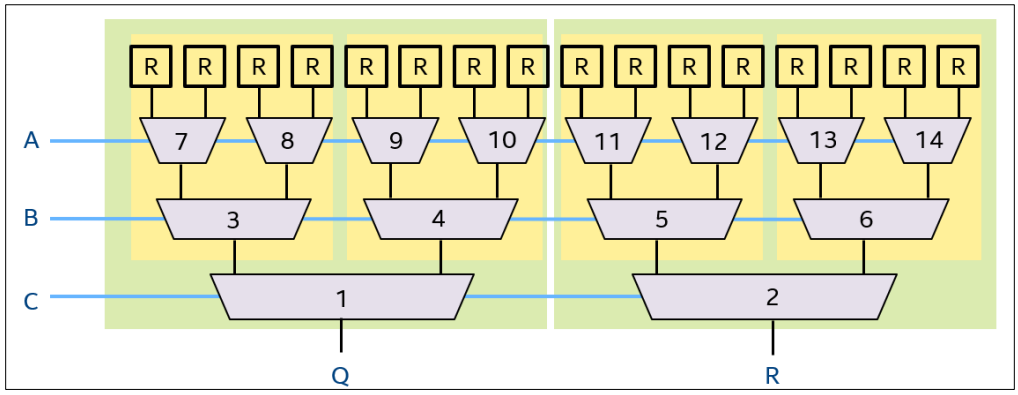
Iida attempts to rescue his claims from indefiniteness by importing a limitation into the plain and ordinary meaning of "LUT units." He argues that "units" must be "irreducible." That is, a "LUT unit" cannot be divided into smaller LUT units. Even if the idea of an "irreducible" circuit component were not nonsensical, *see supra* p. 6, it is an unsupported attempt to rewrite the claims.

As Intel has explained (Dkt. 51 at 19), the word "units" refers to the individual parts into which a collective might be divided. An "apartment building" can be divided into "apartment units," a "measurement" can be divided into "measurement units," and as the patent describes, a "look up table" can be divided into "LUT units." *See* Dkt. 51 at 19. Nothing about this plain and ordinary meaning requires the "units" to be ***irreducible*** parts of the larger whole. A "unit" may or may not be irreducible; it all depends on the context. The metric system for measuring distance is illustrative: it is a system of units, each of which is further reducible. A kilometer is a unit that can

be logically reduced into meters, each of which is further reducible into centimeters, each of which is further reducible into millimeters, each of which is further reducible into micrometers, and so on. A claim limitation that recites a "length unit" would be satisfied by any of these metric units, unless the claim provides additional context that limits the term to a specific unit of measurement. The word "unit," alone, does not connote irreducibility.

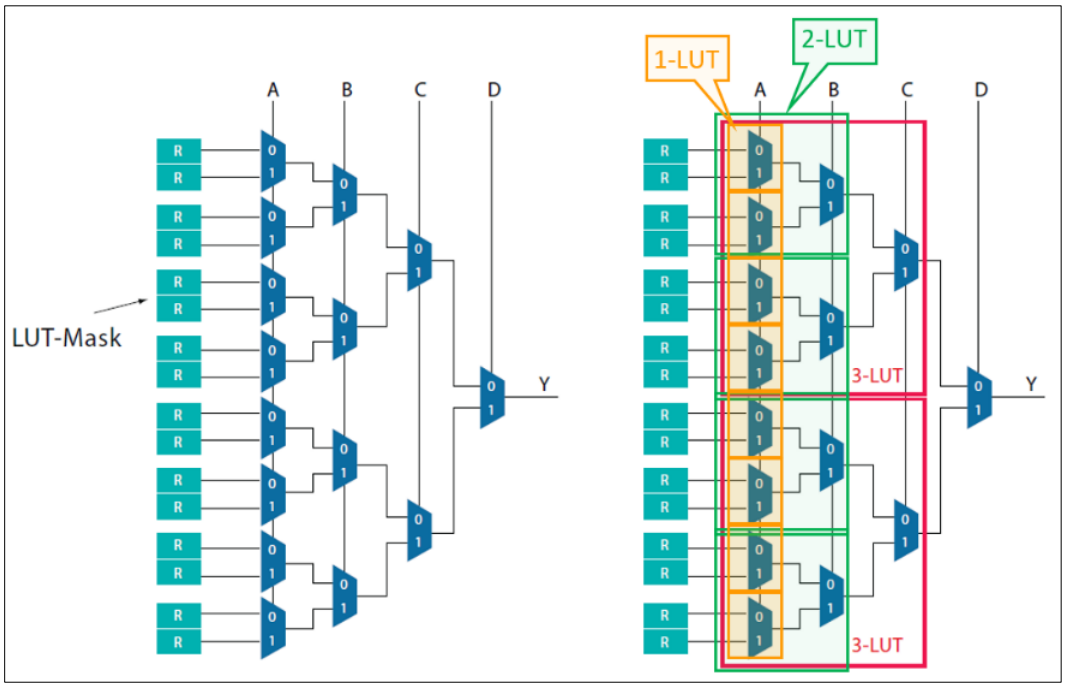
Iida provides another example. Dkt. 54 at 19. As he defines it, an "apartment unit" must have "a kitchen ***and*** a bathroom." *Id.* Using this definition, a two-bedroom apartment with one bathroom and one kitchen cannot be divided into two "apartment units." *Id.* Employing the exact same definition, however, a two-bedroom apartment that has two bathrooms and two kitchens ***could*** be reduced into two "apartment units." As Iida recognizes, it all depends on the "floor plan" of the building, and there must be "sufficient detail" in that floor plan to assess reducibility. *Id.*

Similarly, in the context of the patent, the phrase "LUT units" does not suggest irreducibility. To start, nothing about the meaning of "LUT" requires the "LUT units" be irreducible. In fact, a feature of look up tables is that they often can be viewed as a collection of smaller look up tables. *See* Dkt. 51-1 (Melvin Decl.) ¶ 41. That is, depending on its structure, a look up table can be divided into smaller look up tables. For example, consider again this 3-input (A, B, C), 2-output (Q, R) look up table from Intel's opening brief:



This look up table could be viewed as two 3-input, 1-output look up tables (green boxes) or four 2-input, 1-output look up tables (yellow boxes). Often, as this shows, look up tables can be iteratively divided into smaller and smaller look up tables—quite like metric units of measurement.

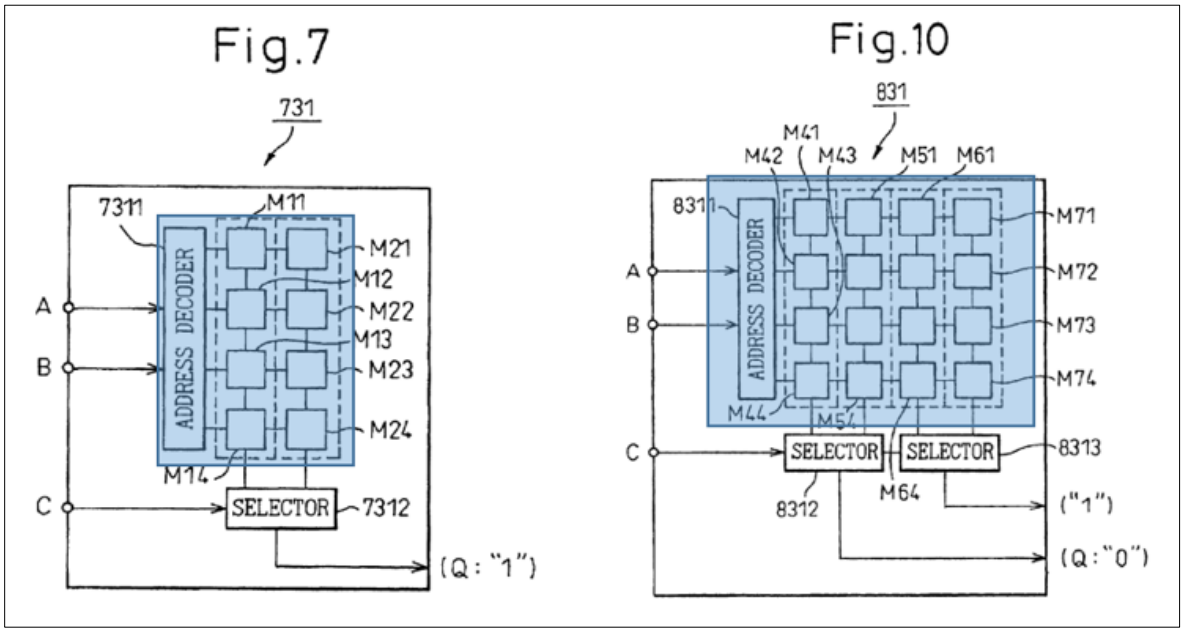
As another example, consider the figure below, which was reproduced in Iida's preliminary infringement contentions (Ex. 20 at 24, 33). The 4-input look up table on the left, which is made up of a tree of multiplexers, also can be "built from" two 3-LUT units (red boxes in original right figure), four 2-input LUT units (green boxes), or eight 1-input LUT units (yellow boxes):



Ex. 19 at 3 & Fig. 2 (annotated). Because there is no physical difference between the left and right figures, "building" the 4-LUT in multiple ways amounts to nothing more than arbitrarily defining the "LUT units" in this figure, and nothing in the patent limits that arbitrary box-drawing exercise.

In fact, some of the '737 patent's preferred embodiments of a "LUT unit" are further reducible, demonstrating that Iida's narrowing definition is inconsistent with the patent specification. For example, the patent states that "FIG. 7 is a block diagram showing an example of 3-input 1-output ***LUT unit***" and "FIG. 10 is a block diagram showing an example of 3-input 2-

output ***LUT unit***." '737 patent at 3:17–18, 3:25–26 (emphasis added). Yet, both "LUT units" can be reduced into smaller LUT units (blue boxes below), making FIG. 7 a 2-input, 2-output "LUT unit" and FIG. 10 a 2-input, 4-output "LUT unit." Thus, requiring "LUT units" to be irreducible would exclude these preferred embodiments. *Dow Chem. Co. v. Sumitomo Chem. Co.*, 257 F.3d 1364, 1378 (Fed. Cir. 2001) ("[A] claim construction that excludes a preferred embodiment is rarely, if ever, correct.") (cleaned up).



In short, Iida is attempting to craft a limitation from whole cloth in an attempt to avoid indefiniteness. Nothing about the plain language of "LUT unit" requires irreducibility, and adopting such a limitation would exclude preferred embodiments. Worse still, the concept of "irreducible" circuit components is itself nonsensical. To be sure, claims should be interpreted to preserve validity ***where possible***, but that is simply not possible here. Iida's construction is unsupported, and it would not preserve validity.

III. CONCLUSION

For the foregoing reasons, Intel respectfully requests that the Court hold that all asserted claims are indefinite or, in the alternative, that the Court adopt Intel's proposed constructions.

Respectfully submitted,

Date: February 23, 2023

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record are being served with a copy of the foregoing sealed documents via electronic mail and publicly filed documents via the Court's CM/ECF system on February 23, 2023.

/s/ Heather E. Takahashi
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